

# **Exhibit A to Response to Office Action**

Response to Office Action

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**CS152**  
**Computer Architecture and Engineering**

**Lecture 5: Cost and Design**

**September 10, 1997**

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**lecture slides: <http://www-inst.eecs.berkeley.edu/~cs152/>**

cs 152 L5 Cost.1

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## Review: Performance and Technology Trends

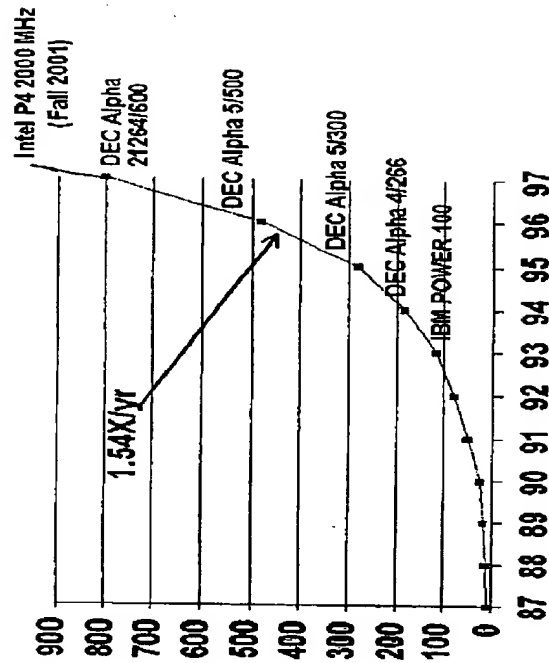
### Technology Power: $1.2 \times 1.2 = 1.7 \times$ / year

- Feature Size: shrinks 10% / yr. => Switching speed improves 1.2 / yr.
- Density: improves 1.2x / yr.
- Die Area: 1.2x / yr.

### The lesson of RISC is to keep the ISA as simple as possible:

- Shorter design cycle => fully exploit the advancing technology (~3yr)
- Advanced branch prediction and pipeline techniques
- Bigger and more sophisticated on-chip caches

### Technology Trends: Processor Performance



Processor performance increase/year,  
referred to as Moore's Law (transistors/chip)



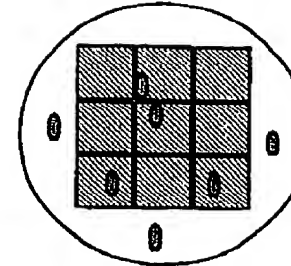
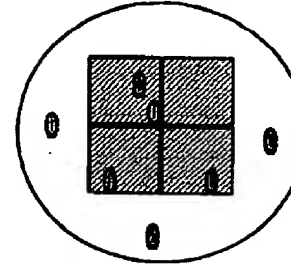
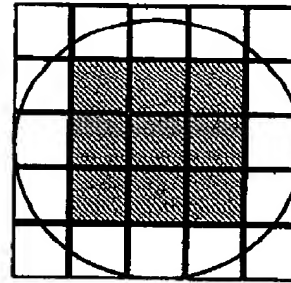
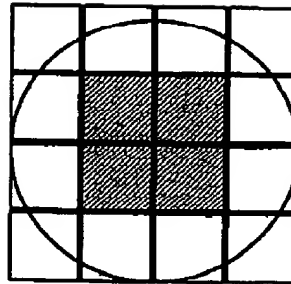
CS 152 L5 Introduction & Number Representation (7)

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# Integrated Circuit Costs

$$\text{Die cost} = \frac{\text{Wafer cost}}{\text{Dies per Wafer} * \text{Die yield}}$$

$$\text{Dies per wafer} \sim \text{eff } \frac{\text{Wafer Area}}{\text{Die Area}}$$



$$\text{Die Yield} = \frac{\text{Wafer yield}}{\left\{ 1 + \frac{\text{Defects\_per\_unit\_area} * \text{Die\_Area}}{?} \right\}}$$

*Die Cost is goes roughly with the cube of the area.*

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